

DEC 0 7 2001

### **POWER OF ATTORNEY BY ASSIGNEE**

The undersigned assignee of the entire interest in the patent applications and issued patents dentified in the attached Exhibit A, by virtue of that certain assignment agreement dated November 27, 2000 by and among BAE Systems Information and Electronic Systems Integration, Inc. and Lockheed Martin Corporation, elects to conduct the prosecution of the patent applications and maintenance of the patents to the exclusion of the inventor(s) and earlier assignees.

The undersigned hereby declares that he has reviewed the above-referenced assignment and hereby declares that, to the best of his knowledge, title is in the Assignee, and further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true. The assignee hereby revokes any previous powers of attorney and appoints the following attorneys, all of Swidler Berlin Shereff Friedman, LLP, to prosecute the patent applications and maintain the patents listed in the attached Exhibit A and transact all business in the Patent and Trademark Office connected therewith:

Edward A. Pennington 32,588	John P. Moran	30,906
Michael A. Schwartz 40,161	Robert C. Bertin	41,488
Alicia A. Meros 44,937	Chadwick A. Jackson	46,495
Sean P. O'Hanlon 47,252	Eric J. Franklin	37,134

Please send all written communications to:

Edward A. Pennington Swidler, Berlin, Shereff, Friedman, L.L.P. 3000 K Street, Washington, D.C. 20007 Fax (202) 295-8478

Please direct all telephone calls to: Robert C. Bertin, 202-424-7872.

ASSIGNEE

BAE SYSTEMS INFORMATION AND ELECTRONIC SYSTEMS INTEGRATION, INC.

Date: November 15, 200/

Kevin M. Perkins

Title: Vice President and Secretary-

Company General Counsel for its IEWS business

### **EXHIBIT A**

27-Jun-1996   5,915,082   22-Jun-1999   25-Jun-1999   25-Jun-1998   25-Jun-1999   25-Jun-1998   25-Jun-1999   25	Title:	Application Number:	Filing Date:	Patent Number:	Issue Date:
Lockstep Processor Systems Process To Personalize Master Slice Wafers And Fabricate High Density VLSI Components With A Single Masking Step Gaut Tolerant MOSFET Driver Gaut Tolerant MOSFET Driver Gaut Tolerant MOSFET Driver  OB/733080  16-Oct-1996  5,796,274  18-Aug-1998  36-Mar-1997  6,034,399  07-Mar-2000  18ilicon-On-Insulator  18ing Domains For Bandwidth Sharing OB/812184  O6-Mar-1997  5,901,148  O4-May-1999  5,970,095  19-Oct-1999  5,970,095  19-Oct-1999  5,970,095  19-Oct-1999  5,867,479  02-Feb-1999  5,867,479  02-Feb-1999  5,867,479  02-Feb-1999  6,188,874B1  13-Feb-2001  08/884675  08/987016  08/987016  08/987016  08/987016  08/989463  12-Dec-1997  6,052,606  18-Apr-2000  18-Apr-2000  18-Apr-2000  18-Jun-1998  6,127,879  03-Oct-2000  Circuit  Digital Multi-Channel  OP/030902  26-Feb-1998  6,091,704  18-Jul-2000  18-Jul-2000  Circuit  Digital Multi-Channel  OP/325641  OP/325645  O4-Jun-1999  6,065,135  16-May-2000  16-Mar-1999  6,065,135  16-May-2000  16-Mar-1999  6,065,135  16-May-2000  16-Jun-1999  6,073,080  16-Jun-1999  6,073,080  16-Jun-1999  6,065,135  16-May-2000  16-Jun-1999  6,065,135  16-May-2000  16-Jun-1999  11-Jun-1999  11-					22-Jun-1999
Process To Personalize Master Slice Wafers And Fobricate High Density VLSI Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Step Pault Tolerant MoSFET Driver Using Components With A Single Masking Step Pault Tolerant MoSFET Driver Masking Step Pault Tolerant MoSFET Driver Driver Tolerant MoSFET Driver Masking Step Pault Tolerant MoSFET Driver Driver Tolerant MoSFET Driver Driver Driver Tolerant Driver	<del>-</del> ,				
And Fabricate High Density VLSI Components With A Single Masking Step Pault Tolerant MOSET Driver  Bilectrostatic Discharge Protection For D8/733080 16-Oct-1996 5,796,274 18-Aug-1998 18-Bectrostatic Discharge Protection For D8/812183 06-Mar-1997 5,901,148 04-May-1999 18-Decure Data Transmission On A TDM 08/837165 14-Apr-1997 5,901,148 04-May-1999 19-Oct-1999 19-Oc	Process To Personalize Master Slice Wafers	08/728880	10-Oct-1996	5,858,817	12-Jan-1999
Components With A Single Masking Step Fault Tolerant MOSFET Driver O8/733080 16-Oct-1996 5,796,274 18-Aug-1998 Silleon-On-Insulator Ring Domains For Bandwidth Sharing O8/812184 O6-Mar-1997 S,901,148 O4-May-1999 Secure Octo Transmission On A TDM Secure Octo Transmission On A TDM Secure Octo Transmission On A TDM O8/837165 O8/884650 O7-Jun-1997 S,970,095 O7-Jun-1997 S,970,095 O7-Jun-1999 Secure Octo Transmission On A TDM O8/884650 O7-Jun-1997 S,867,479 O2-Feb-1999 Control And Telemetry Signal Communication System For Geostationary Systellites Shallow Isolation Trench Forming Process For Sillcon-On-insulator Technology Reversible Keypad And Display For A Isolation Individual Color					
Country   Coun					
Silicon-On-Insulator Ring Domains For Bandwidth Sharing  08/812184  06-Mar-1997  5,901,148  04-May-1999  Secure Data Transmission On A TDM sochronous Network Digital Multi-Channel Demutiplexer/Multiplex (MCD/M Architecture) Control And Telemetry Signal Communication System For Geostationary Statellities Shallow Isolation Trench Forming Process For Silicon-On-Insulator Technology Reversible Keypad And Display For A Elephone Handset Integrated Circuit Package And Method ancreasing Density Of I/O Leads Multi-Channel Demutiplexer/Multiplexer (MCD/M) Architecture Fror Detection And Fault Isolation For Lockstep Process Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Sofellite Telephone Handset Enhanced Single Event Upset Immune Lock Spligle Isonal Clack Splitter Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Method And Apparatus For A SEU T	Fault Tolerant MOSFET Driver	08/733080	16-Oct-1996	5,796,274	18-Aug-1998
Silicon-On-Insulator Ring Domains For Bandwidth Sharing  08/812184  06-Mar-1997  5,901,148  04-May-1999  Secure Data Transmission On A TDM sochronous Network Digital Multi-Channel Demutiplexer/Multiplex (MCD/M Architecture) Control And Telemetry Signal Communication System For Geostationary Statellities Shallow Isolation Trench Forming Process For Silicon-On-Insulator Technology Reversible Keypad And Display For A Elephone Handset Integrated Circuit Package And Method ancreasing Density Of I/O Leads Multi-Channel Demutiplexer/Multiplexer (MCD/M) Architecture Fror Detection And Fault Isolation For Lockstep Process Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Sofellite Telephone Handset Enhanced Single Event Upset Immune Lock Spligle Isonal Clack Splitter Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Method And Apparatus For A SEU T	Flectrostatic Discharge Protection For	08/812183	06-Mar-1997	6.034.399	07-Mar-2000
Ring Domains For Bandwidth Sharing 08/812184 06-Mar-1997 5,901,148 04-May-1999 Secure Data Transmission On A TDM 08/837165 14-Apr-1997 5,970,095 19-Oct-1999 Sochronous Network 02-Digital Multi-Channel 08/884650 27-Jun-1997 5,867,479 02-Feb-1999 Demultiplexer/Multiplex (MCD/M Architecture) 08/884650 27-Jun-1997 5,867,479 02-Feb-1999 Control And Telemetry Signal 08/884675 27-Jun-1997 6,188,874B1 13-Feb-2001 Communication System For Geostationary 3citellities 3-Brailow Isolation Trench Forming Process 6-For Silicon-On-insulator Technology 7-For Silicon-On-insulator Technology 8-Portable Keypad And Display For A 16-Independent Handset 16-Independent Plandset 16-Inde				0,55 4,511	
sochronous Network Digital Multi-Channel Demultiplexer (McD/M Architecture) Control And Telemetry Signal Communication System For Geostationary Signalitellites Shallow Isolation Trench Forming Process For Silicon-On-Insulator Technology Reversible Keypad And Display For A Ielephone Handset Integrated Circuit Package And Method Increasing Density Of I/O Leads Multi-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Redicition Hardened Six Transistor Random Access Memory And Memory Device Sofellite Telephone Handset Enhanced Single Event Upset Immune Lotch Circuit In Silu Proximity Gap Monitor For Upset (SEU) Tolerant Clock Spillter Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Digital Mathod And Apparatus For A SEU Tolerant Dig/559661 D9/559661 D9/559661 D9/559661 D9/559661 D9/559661 D9/559061 D9/559660 D8/884650 D9-Jun-1997 D9-Ba, 867,479 D9-Pec-1997 D9-Dec-1997 D9-	Ring Domains For Bandwidth Sharing	08/812184	06-Mar-1997	5,901,148	04-May-1999
sochronous Network Digital Multi-Channel Demultiplexer (McD/M Architecture) Control And Telemetry Signal Communication System For Geostationary Signalitellites Shallow Isolation Trench Forming Process For Silicon-On-Insulator Technology Reversible Keypad And Display For A Ielephone Handset Integrated Circuit Package And Method Increasing Density Of I/O Leads Multi-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Redicition Hardened Six Transistor Random Access Memory And Memory Device Sofellite Telephone Handset Enhanced Single Event Upset Immune Lotch Circuit In Silu Proximity Gap Monitor For Upset (SEU) Tolerant Clock Spillter Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Digital Mathod And Apparatus For A SEU Tolerant Dig/559661 D9/559661 D9/559661 D9/559661 D9/559661 D9/559661 D9/559061 D9/559660 D8/884650 D9-Jun-1997 D9-Ba, 867,479 D9-Pec-1997 D9-Dec-1997 D9-	Socure Data Transmission On A TDM	08/837165	1/-Anr-1007	5 070 005	10-Oct-1000
Digital Multi-Channel Demultiplexer/Multiplex (MCD/M Architecture) Control And Telemetry Signal Communication System For Geostationary Satellities Shallow Isolation Trench Forming Process For Silicon-On-Insulator Technology Reversible Keypad And Display For A Telephone Handset Integrated Circuit Package And Method Increasing Density Of I/O Leads Multi-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset Enhanced Single Event Upset Immune Latch Circuit In Situ Proximity Gap Monitor For Lithography Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Method And Apparatus For A		00/00/100	14-Api-1777	0,770,070	17-001-1777
Demultiplexer/Multiplex (MCD/M Architecture) Control And Telemetry Signal Cornmunication System For Geostationary Satellites Shallow Isolation Trench Forming Process O8/987016  O9-Dec-1997  6.052.606  18-Apr-2000  16-Jan-1998  16-Jan-1998  16-Jan-1998  16-Jan-1998  6.127,879  03-Oct-2000  Circuit  O9/030902  26-Feb-1998  6.127,879  03-Oct-2000  Circuit  O9/325641  O4-Jun-1999  6.091,704  18-Jul-2000  Demultiplexer/Multiplexer (MCD/M)  Architecture  Error Detection And Fault Isolation For O9/325645  O4-Jun-1999  6.011,780  29-Aug-2000  Access Memory And Memory Device  Satellite Telephone Handset  O9/384429  27-Aug-1999  Enhanced Single Event Upset Immune O9/480454  11-Jan-2000  6.275,080  14-Aug-2001  In Situ Proximity Gap Monitor For Uthography  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant O9/559661  28-Apr-2000  28-Apr-2000		08/884650	27-Jun-1997	5 867 479	02-Feb-1999
Architecture) Control And Telemetry Signal Communication System For Geostationary Statellites Shallow Isolation Trench Forming Process Isolation Interest Isolation For		00/004000	2, 00,	0,007,477	02:00
Control And Telemetry Signal Communication System For Geostationary Statellites Shallow Isolation Trench Forming Process For Silicon-On-Insulator Technology Reversible Keypad And Display For A Ielephone Handset Integrated Circuit Package And Method Increasing Density Of I/O Leads Multi-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset Enhanced Single Event Upset Immune Lotch Circuit Distriction For Lotch Circuit Distriction For A Single Event Upset (SEU) Tolerant Clock Splitter Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Method And Apparatus For A SEU Tolerant Method And Apparatus For A SEU Tolerant Delection For Single Event Upset Increase Method And Apparatus For A SEU Tolerant Delection For Defection And Apparatus For A SEU Tolerant Delection For Defection And Apparatus For A SEU Tolerant Delection For Defection And Fault Isolation For Defection And Memory Device Defending Floric Processor Systems Delection For Defection And Fault Isolation For Defection And Fault Isolation For Defection And Memory Device Defending Floric Processor Systems Defending F			]		
Communication System For Geostationary Satellites Sinciliow Isolation Trench Forming Process For Silicon-On-Insulator Technology Reversible Keypad And Display For A Telephone Handset Relephone		08/884675	27-Jun-1997	6,188,874B1	13-Feb-2001
Satellites Shallow Isolation Trench Forming Process For Sillcon-On-Insulator Technology Reversible Keypad And Display For A Telephone Handset Integrated Circuit Package And Method Increasing Density Of I/O Leads Multil-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset Integrated Circuit O9/325645 O4-Jun-1998 O4-Jun-1999 O4-Jun-1999 O5-055,080 O4-Jun-1999 O5-055,080 O5-052.606 O	Communication System For Geostationary				
For Silicon-On-Insulator Technology Reversible Keypad And Display For A Telephone Handset Telephone Ha	Satellites				
Reversible Keypad And Display For A Telephone Handset Integrated Circuit Package And Method Increasing Density Of I/O Leads Multi-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset Enhanced Single Event Upset Immune Lotch Circuit In Silu Proximity Gap Monitor For Uthorid Filp Flop Method And Apparatus For A Single Event Method And Apparatus For A Scannable Hybrid Filp Flop Method And Apparatus For A SEU Tolerant Dig/007980 Ita-Jan-1999 Ita-Jan-2000 Ita-Jan-1998 Ita-Jan-1998 Ita-Jan-1998 Ita-Jan-1998 Ita-Jan-1998 Ita-Jan-1998 Ita-Jan-1998 Ita-Jan-1998 Ita-Jan-1999 Ita-Jan-1999 Ita-Jan-1999 Ita-Jan-2000 Ita-Jan-2000 Ita-Jan-1999 Ita-Jan-2000 Ita-Jan-1999 Ita-Jan-2000 Ita-Jan-2000 Ita-Jan-1999 Ita-Jan-2000 Ita-Jan-1999 Ita-Jan-2000 Ita	Shallow Isolation Trench Forming Process	08/987016	09-Dec-1997		
Telephone Handset Integrated Circuit Package And Method Increasing Density Of I/O Leads Multi-Channel Overvoitage Protection Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Statellite Telephone Handset Enhanced Single Event Upset Immune Lot Circuit In Situ Proximity Gap Monitor For Uthography Method And Apparatus For A Single Event Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Method An	For Sillcon-On-Insulator Technology				
Integrated Circuit Package And Method Increasing Density Of I/O Leads Multi-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Enhanced Single Event Upset Immune Lotch Circuit In Sith Proximity Gap Monitor For Uthor And Apparatus For A Single Event Upset (SEU) Tolerant Clock Spillter Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant		08/989463	12-Dec-1997	6.052.606	18-Apr-2000
Multi-Channel Overvoltage Protection Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Sotellite Telephone Handset In Situ Proximity Gap Monitor For Uttory Wethod And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant O9/559661  09/030902 26-Feb-1998 6.127,879 03-Oct-2000 04-Jun-1999 6.091,704 18-Jui-2000 04-Jun-1999 6.065,135 16-May-2000 04-Jun-1999 6.111,780 29-Aug-2000 09/325645 04-Jun-1999 6.111,780 29-Aug-2000 11-Jan-2000 6.275,080 14-Aug-2001 10-Feb-2000 09/559659 28-Apr-2000 28-Apr-2000 28-Apr-2000 28-Apr-2000	Telephone Handset				<u> </u>
Multi-Channel Overvoltage Protection Circuit  Digital Multi-Channel Demultiplexer (MCD/M) Architecture  Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device  Satellite Telephone Handset  Enhanced Single Event Upset Immune Lotch Circuit In Situ Proximity Gap Monitor For Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant  09/559661  09/559660  09/559661  00-Feb-1998  6.027,879  6.091,704  18-Jui-2000  6.065,135  16-May-2000  04-Jun-1999  6.065,135  16-May-2000  04-Jun-1999  6.011,780  29-Aug-2000  10-Feb-2000  11-Jan-2000  6.275,080  14-Aug-2001  10-Feb-2000  10-Feb-2000  28-Apr-2000  28-Apr-2000  10-Feb-2000  28-Apr-2000  28-Apr-2000  10-Feb-2000  1		09/007980	16-Jan-1998		
Circuit Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset Enhanced Single Event Upset Immune Latch Circuit In Silu Proximity Gap Monitor For Uthography Method And Apparatus For A Single Event Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant Method And Method And Apparatus For A SEU Tolerant Method And Method And Apparatus For A SEU					
Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset U9/384429 Enhanced Single Event Upset Immune Lotch Circuit In Situ Proximity Gap Monitor For Uthography Method And Apparatus For A Single Event Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant U9/559661 U9/559661 U9/559661 U9/559661 U9/559661 U9/559660		09/030902	26-Feb-1998	6.127,879	03-Oct-2000
Demultiplexer/Multiplexer (MCD/M) Architecture  Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Safellite Telephone Handset  Enhanced Single Event Upset Immune Latch Circuit In Situ Proximity Gap Monitor For Lithography Method And Apparatus For A Single Event Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant D9/559651  D9/559661  D9/559661  D9/559661  D4-Jun-1999  6,111,780  29-Aug-2000  4,065,135  D4-Jun-1999  6,111,780  29-Aug-2000  4,11-Jan-2000  6,275,080  14-Aug-2001  10-Feb-2000  28-Apr-2000  28-Apr-2000  28-Apr-2000  28-Apr-2000  28-Apr-2000  28-Apr-2000					
Architecture  Error Detection And Fault Isolation For Lockstep Processor Systems  Radiation Hardened Six Transistor Random Access Memory And Memory Device  Satellite Telephone Handset  Enhanced Single Event Upset Immune Latch Circuit In Situ Proximity Gap Monitor For Lithography  Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant  D9/559661  09/559661  09/559661  09/559661  09/559661  09/559661  09/559660  09/559660  09/559660  09/559660  09/559660  09/559660  09/559660  09/559660  28-Apr-2000  28-Apr-2000		09/241313	01-Feb-1999	6,091,704	18-Jul-2000
Error Detection And Fault Isolation For Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset  Enhanced Single Event Upset Immune Latch Circuit In Situ Proximity Gap Monitor For Uthography Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A SEU Tolerant Method Security Method And Apparatus For A SEU Tolerant Method Security Method Sec					
Lockstep Processor Systems Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset  Enhanced Single Event Upset Immune Latch Circuit In Situ Proximity Gap Monitor For Uthography  Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant  D9/559661  D4-Jun-1999  6,111,780  29-Aug-2000  11-Jan-2000  6,275,080  14-Aug-2001  10-Feb-2000  28-Apr-2000  28-Apr-2000  28-Apr-2000  28-Apr-2000		00/205443	04 1 1000	4.045.125	14 May 2000
Radiation Hardened Six Transistor Random Access Memory And Memory Device Satellite Telephone Handset  Enhanced Single Event Upset Immune Latch Circuit In Situ Proximity Gap Monitor For Lithography  Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant D9/559661  09/559661  04-Jun-1999  6,111,780  29-Aug-2000  11-Jan-2000 6,275,080  14-Aug-2001  10-Feb-2000  28-Apr-2000  28-Apr-2000  28-Apr-2000		U9/325041	104-Jun-1999	0,000,130	10-1VIQY-2000
Access Memory And Memory Device Satellite Telephone Handset  Enhanced Single Event Upset Immune Latch Circuit In Situ Proximity Gap Monitor For Lithography Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter Method And Apparatus For A Scannable Hybrid Flip Flop Method And Apparatus For A SEU Tolerant		00/325645	04- luo-1000	6 111 780	20-447-2000
Enhanced Single Event Upset Immune		07/323043	04-3011-1999	0,111,700	27-Aug-2000
Enhanced Single Event Upset immune Latch Circuit In Situ Proximity Gap Monitor For Lithography  Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable Hybrid Filip Flop  Method And Apparatus For A SEU Tolerant		09/384429	27-Aug-1999		<del></del> . <u></u>
Latch Circuit In Situ Proximity Gap Monitor For Uthography  Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant Up/559661			<u> </u>		
In Situ Proximity Gap Monitor For Lithography  Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant		09/480454	11-Jan-2000	6,275,080	14-Aug-2001
Lithography  Method And Apparatus For A Single Event 09/559659 28-Apr-2000  Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable 09/559660 28-Apr-2000  Hybrid Filip Flop  Method And Apparatus For A SEU Tolerant 09/559661 28-Apr-2000		00.4500=+0		ļ	
Method And Apparatus For A Single Event U9/559659 28-Apr-2000  Upset (SEU) Tolerant Clock Splitter 28-Apr-2000  Method And Apparatus For A Scannable U9/559660 28-Apr-2000  Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant U9/559661 28-Apr-2000	•	09/502062	10-Feb-2000		
Upset (SEU) Tolerant Clock Splitter  Method And Apparatus For A Scannable 09/559660 28-Apr-2000  Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant 09/559661 28-Apr-2000	urnography	00/550/50	00.4		<b></b>
Method And Apparatus For A Scannable 09/559660 28-Apr-2000  Hybrid Filip Flop  Method And Apparatus For A SEU Tolerant 09/559661 28-Apr-2000		104/224624	28-Apr-2000		
Hybrid Flip Flop  Method And Apparatus For A SEU Tolerant 09/559661 28-Apr-2000	• • •	00/550/70	00 474 0000	<del> </del>	<del> </del>
Method And Apparatus For A SEU Tolerant 09/559661 28-Apr-2000		04/254000	28-Apr-2000		
		00/660443	00 0000	<del>- </del>	<del> </del>
	Method And Apparatus For A SEU Tolerant Clock Splitter	וססצפפוצען	20-Apr-2000		



Title:	Application Number:	Filing Date:	Patent Number:	Issue Date:
Distributed Determination Of Explicit Rate In An ATM Communication System	09/570050	12-May-2000		
Self-Equalized Low Power Precharge Sense Amp For High Speed SRAMs	09/570064	12-May-2000		
Tool Suite For The Rapid Development Of Advanced Standard Cell Libraries	09/597229	20-Jun-2000		
Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture	09/625641	25-Jul-2000	7 4	
Elimination Of Narrow Device Width Effects In Complementary Metal Oxide Semiconductor (CMOS) Devices	09/741028	21-Dec-2000		
Ball Grid Array (BGA) To Column Grid Array (CGA) Conversion Process	09/774010	31-Jan-2001		
Polyphase-Discrete Fourler Transform (DFT) Sub-band Definition Filtering Architecture	09/780348	12-feb-2001		
Method And Apparatus For A Radiation Hardened Clock Splitter	09/838131	20-Apr-2001		

### PATENT ASSIGNMENT

THIS PATENT ASSIGNMENT is made and entered into as of the 27th day of November 2000, between Lockheed Martin Corporation, a Maryland corporation ("Assignor"), and BAE SYSTEMS INFORMATION AND ELECTRONIC SYSTEMS INTEGRATION INC. (formerly known as BAE SYSTEMS Sanders Inc.), a Delaware corporation ("Assignee").

## WITNESSETH:

WHEREAS, Assignor is the owner of the entire right, title and interest in and to all of the patents and patent applications set forth on Schedule A annexed hereto and made a part hereof and has the unrestricted right to sell, assign and transfer such patents and patent applications; and

WHEREAS, pursuant to the terms of a Transaction Agreement, dated as of July 13, 2000, by and among Assignor, Assignee and BAE SYSTEMS North America Inc., a Delaware corporation, Assignor has agreed, among other things, to transfer to Assignee said patents and patent applications;

NOW. THEREFORE, in consideration of the sum of ten (\$10.00) dollars and other good and valuable consideration paid by Assignee to Assignor, the receipt and sufficiency of which is hereby acknowledged, Assignor hereby sells, assigns, transfers and sets over to Assignee, its successors and permitted assigns, Assignor's entire right, title and interest in and to the patents and patent applications set forth on Schedule A hereto, including (without limitation) all divisions, reissues, substitutions, continuations and extensions thereof, all priority rights under the International Convention for the Protection of Industrial Property for every member country (and any other international convention or treaty), any and all Letters Patent and reissues and extensions of Letters Patent granted thereon and any and all rights corresponding to any of the foregoing throughout the world and any and all accounts, contract rights, warranties, litigation claims and rights, including the right to sue for and collect upon all claims for profits and damages as a result of past infringement, if any, and other general intangibles of Assignor related to any of the foregoing, in each case whether now existing or hereafter acquired or created, whether owned, leased or licensed beneficially or of record and whether owned, leased or licensed individually, jointly or otherwise, together with the products and proceeds thereof (including license royalties and the proceeds of infringement suits), all payments and other distributions with respect thereto and any divisions, reissues, substitutions, continuations and extensions of any and all of the foregoing (all of the foregoing herein collectively referred to as the "Patents").

Assignor further agrees that it shall on the date hereof and from time to time thereafter, at the request of Assignee, perform or cause to be performed such acts and execute, acknowledge and deliver at the request of Assignee, such documents as may reasonably be required to evidence or effectuate the sale, conveyance, assignment, transfer and delivery to Assignee of the Patents or for the performance by Assignor of any of its obligations hereunder.

IN WITNESS WHEREOF, Assignor has executed this Patent Assignment as of the date above written.

LOCKHEED MARTIN CORPORATION

By:

Name: Wowerw. Lo

Title: Director, Business Ventur

BAE SYSTEMS INFORMATION AND ELECTRONIC SYSTEMS INTEGRATION INC.

Bv:

Name: Earle o murn.

Title: Viciproydent

# DISTRICT OF COLUMBIA ss.:

On the 27th day of November, 2000, before me personally can warren w. Lanning, to me known (or satisfactorily proven), who being to me duly sworn, did depose and say that he is the Drycetor, Busines Vertucas
instrument, and that he was fully authorized to execute this Patent Assignment on behalf of sai
Notary Public Notary
My Comment
DISTRICT OF COLUMBIA ss.:
On the 2Th day of November, 2000, before me personally cam temporal to me known (or satisfactorily proven), who being by
me duly sworn, did depose and say that he is the Vice Report and Scerebook BAE SYSTEMS Information and Electronic Systems Integration Inc., the corporation described in, and which executed the foregoing instrument, and that he was fully authorized to execute this Patent Assignment on behalf of said corporation.
Liss a Charge
Notar Public

# SCHEDULE A

# LM Space Electronics & Communications

CaseNumber Title	er Title	Country Status	Status	Tare Day			
FE-00003	High Density Integrated Circuit			riie Dale	rue Date Applyumb	Issue Date	Issue Date PatNumber
FE-00006	US Expi JP Abai Process for Increasing the Immunity of 10° to Ionizing Radiation	US JP izing Radia	Expired Abandone <i>Tion</i>	24-Jan-1979 20-Dec-1979	5946 164876/79	17-Jun-1980 20-Jan-1984	4,200,079
FE-00007	US Secret 28-Jun-1982 FET Read Only Memory Cell With Work Line Augmented Precharging Of Bit Lines	US Rmented Pr	Secret 'echarging C	28-Jun-1982 J'Bit Lines	393,012	,	
FE-00008	Improved Local Oxide Isolation Process	GB GB FR AT US EP	Abandone Granted Granted Granted Granted Granted	15-May-1984 24-Jul-1984 24-Jul-1984 24-Jul-1983 24-Jul-1984 24-Jul-1984	095787/84 84108711.7 84108711.7 084108711.7 534,035 084108711.7	10-Nav-1988 27-Sep-1989 27-Sep-1989 27-Sep-1989 16-Feb-1988 27-Sep-1989	1464935 0135699 0135699 4,725,986 0135699
		Sn	Secret	06-Jul-1984	643,902		

CaseNumber Title FE-00009 High Data	er Title High Density, High Performance, Single Event Upset Immune Data	Country Status pxet Immune	Status ne	File Date	File Date ApplNumb	Issue Date	Issue Date PatNumber
	·	SN	Granted	09-Mar-1987	23,426	10-Jan-1989	4 797 804
		FR	Granted	22-Jan-1988	88100947.6	13-Jan-1993	281 741
		Ę,	Granted	20-Jan-1988	008597/88	07-Oct-1994	1878682
		EP	Granted	22-Jan-1988	88100947.6	13-Jan-1993	281 741
		68	Granted	22-Jan-1988	88100947.6	13-Jan-1993	281 741
	,	DE	Granted	22-Jan-1988	88100947.6	13-Jan-1993	3877381308
r.E-00010	Parity Generator Circuit And Method				`		
		ЕР	Pending	23-Jan-1989	89101069.6		
		ns	Granted	17-Feb-1988	156,626	07-Nov-1989	4 879 675
		٩	Lapsed	18-Nov-1988	290385/88	14-Oct-1992	0705071
FE-00012	Soft Error Resistant CMOS Data Cells						6726071
		NS	Granted	31-Mar-1988	176,052	25-Jul-1989	4 R52 OGD
		GB	Lapsed	23-Dec-1988	88121619.6	10-Jun-1992	335,008
		٩	Pending	20-Feb-1989	38541/89		
		DE	Lapsed	23-Dec-1988	88121619.6	10-Jun-1992	3871945208
		F.	Lapsed	23-Dec-1988	88121619.6	10-Jun-1992	355 008
FE-00016	Process for Increasing the Immunity of IC to Ionizing Radiation	zing Radia	tion				
		Sn	Secret	13-Sep-1988	246,136		

PatNumber	419.760 69028169.2 3015084 4.996.670 419.760	481,329 2549221 69117420.2 481,329 5,117,129	5,234,651
Issue Date PatNumber	21-Aug-1996 21-Aug-1996 17-Dec-1999 26-Feb-1991 21-Aug-1996 21-Aug-1996	28-Feb-1996 08-Aug-1996 28-Feb-1996 28-Feb-1996 26-May-1992 28-Feb-1996	02-Dec-1996 10-Aug-1993
File Date ApplNumb	90108357.6 90108357.6 236022/90 414,889 90108357.6 90108357.6	544,140 91117104.9 290475/91 91117104.9 91117104.9 598,300	057624/94 829,667
File Date	03-May-1990 03-May-1990 07-Sep-1990 28-Sep-1999 03-May-1990 03-May-1990 09-Sep-1990	13-Jun-1990 08-Oct-1991 11-Oct-1991 08-Oct-1991 16-Oct-1990 08-Oct-1991	28-Mar-1994 03-Feb-1992
Country Status y Rechindancy	Granted Granted Granted Granted Granted Granted Pending	Secret Granted Granted Granted Granted Granted Granted Granted	Granted ://c·c·t Granted
Standby Power, Radiation Hardened, Memon iit	EP Granted 03-May  DE Granted 03-May  JP Granted 07-Sep  US Granted 28-Sep  GB Granted 03-May  FR Granted 03-May  WO Pending 09-Sep	US Secret 13-Jun CALOS Off Chip Driver for Fault Tolerant Cold Sparing  EP Granted 11-Oct  DE Granted 08-Oct  FR Granted 08-Oct  US Granted 16-Oct  GB Granted 08-Oct  GB Granted 08-Oct  GB Granted 08-Oct  GB Granted 08-Oct	JP Gr Small Cell Low Contact Assistance Rugged Power Field Effect Devices And Method Of Fabrication US Ga
CaseNumber Title FE-00017 Zero Circo	FE-00020	FE-00021	FE-00029

Pake 3 of 20

CaseNumber Title FE-00031 Distr	er Title Distributed Programmable Priority Arbitration	Country Status	Status	File Date	File Date ApplNumb	Issue Date	Issue Date PatNumber
FE-00035	JP US Fast Fourier Transform Using Balanced Coefficients	al US 111.s	Granted Granted	01-Mar-1993 30-Apr-1992	39810/93 876,239	27-Jun-1996 26-Apr-1994	2531918
		ط ط ن	Granted Pending	22-Oct-1991 13-Jun-1991	301336/91 91109688.1	13-Jun-1997	2662124
FE-00040	US An Electrostatic Discharge Protect Diode For Silicon-On- Insulator Technology	us con-On-	Granled	13-Jan-1993	004,217	15-Nov-1994	5,365,469
		٩٢	Granted	28-Mar-1994	6-57668/94	09-May-1997	2647339
		UE	Granled	17-Feb-1994	94102415.0	21-Apr-1999	0622850
		FR	Granted	17-Feb-1994	94102415.0	21-Apr-1999	0622850
		ЕР	Granted	17-Feb-1994	94102415.0	21-Apr-1999	0622850
		GB	Granted	17-Feb-1994	94102415.0	21-Apr-1999	0622850
		Sn	Abandone	30-Apr-1993	056,042		00552830
FE-00041	Method To Prevent Latch-Up And Improve Breakdown Voltage In SOI Masfets	lown Volta	sa				
		EP	Pending	17-Feb-1994	94102414.3		
		ns	Granled	12-Sep-1994	304,639	18-Jun-1996	5,527,724

10 m 100 m 6 2 m 1 m 1 m	A Method Of Forming A Frontside Contact To the Silicon Substrate Of A SOI Wafer					1 anymmer
		Granted	30-Apr-1993	054,992	24-May-1994	5.314.841
J	DE Per	Pending	17-Feb-1994	94102416.8	•	
П	EP Pe	Pending	17-Feb-1994	94102416.8		
7	JP Gra	Granted	18-Apr-1994	078654/94	26-Feb-1999	2801221
0	GB Per	Pending	17-Feb-1994	94102416.8		70107
Fower Bus Digital Communication System	FR Per	Pending	17-Feb-1994	94102416.8		
US Granted 04-Oct-1993 131 Single Even Upset Hardening Of Commercial VLSI Technology Without Circuit Redesign	US Gra Technology	Granted Ry Without	04-Oct-1993 Circuit Redes	131,346 iign	01-Jul-1997	5,644,286
ס	US Pen	Pending	26-Oct-1993	141,505		
q		Abandone	19-Oct-1994	6-253600		
E Method To Radiation Harden The Buried Oxide In Silicon-On-Insulator Structures	EP Pen	Pending	30-Aug-1994	94113502.2		
ח	US Granted	nted	28-Oct-1993	142,030	01-Nov-1994	5 360 752
El Spare Signal Line Switching Method and Apparatus	EP Granted	nled	14-Oct-1994	94116233.1	22-Dec-1999	652591A1
Sn		ited	14-Mar-1994	212,372	05-Sep-1995	5,448,572
, .	Granled	led	26-Jun-1992	168828/92	21-Nov-1996	2113094

CaseNumber Title FE-00070 Gate Devid	Overlapped Lightly Doped Drain For Burice :es	Country Status l Channel	Status	File Date	File Date ApplNumb	Issue Date	Issue Date PatNumber
FE-00071	Current Overland Protection Circuit	GB US FR JP DE EP	Granled Granled Granled Granled Granled	26-May-1994 30-Apr-1993 26-May-1994 04-Jun-1994 26-May-1994 26-May-1994	94108054.1 054,994 94108054.1 6-127422 94108054.1	29-Nov-1995 25-Oct-1994 29-Nov-1995 19-Sep-1997 29-Nov-1995 10-Nov-1999	0684640 5,358,879 684640 2698046 0684640
FE-00072	Single Event Upset Hardened CMOS Latch Circuit	Sn ·	Granled	12-Jan-1995	371,718	, 10-Oct-1995	5,457,591
FE-00073	Lithography	. SI	Granted	01-Feb-1995	382,112	02-Apr-1996	5,504,703
FE-00074	US Single Event Upset Immune Register With Fast Write Access	ie Access u	Granled	17-Feb-1995	389,993	02-Apr-1996	5,504,793
		o sn	Granted	21-Feb-1995	391,798	11-Jun-1996	5,525,923

CaseNumber Title FE-00075 Chec	r Titte Checkpoint Retry Mechanism	Country	Status	File Date	File Date ApplNumb	Issue Date	PatNumber
	·	ns	Abandone	23-Aug-1988	235,345	27-Mar-1990	4.912.707
		ď	Abandone	11-Aug-1989	0207115	07-Apr-1995	1922412
		GB	Abandone	08-Jun-1989	89110329.3	13-Aug-1995	0355286
		DE	Abandone	08-Jun-1989	89110329.3	13-Aug-1995	0355286
		F	Abandone	08-Jun-1989	89110329.3	13-Aug-1995	0355286
		EP	Abandone	08-Jun-1989	89110329.3	13-Aug-1995	0355286
FE-00090	Efficient Dual Source Fault Tolerant Power Controller	roller				•	
FE-00091	US A Scaleable, Radiation Hardened Shallow Trench Isolation	US I <i>Isolation</i>	Granted	16-Nov-1995	559,584	28-Jan-1997	5,598,041
		Sn	Abandone	01-Jul-1999	60/142,035		
FE-00092	US Apparatus And Method For Cooling Standard Electronic Modules	us retronic	Pending	30-Jun-2000			
FE-00101	US Abandone Error Detection and Fault Isolation For Lockstep Processor Systems	us Processor	Abandone Systems	19-Jan-1996	588,804		
FE-00107	X-Ray Mask Pellicle	S n	Granted Granted	07-Jun-1996 04-Jun-1999	325,641	22-Jun-1999 16-May-2000	5,915,082 6,065,135
		Sn	Granled	06-Sep-1996	716,657	11-Aug-1998	5,793,836

Tuesday, November 21, 2000

Page 7 of 20

•
=
œ
٠
2
•

CaseNumber Tidle FE-00113 Proc High	ess To Personalize Master Slice Wafer And F Density VLSI Components With A Single Ma	Country Status abricate	File Date	File Date ApplNumb	Issue Date	Issue Date - PatNumber
FE-00114		Granled	10-Oct-1996	728,880	12-Jan-1999	5,858,817
FE-00115	US G Lithographic Patterning Method And Mask Set Therefor With Light Field Trim Mask	Granted r. IVith	16-Oct-1996	733,080	18-Aug-1998	5.796,274
FE-00121	US Ring Domains For Bandwidth Sharing	Granled	31-Ocl-1996	740,598	15-Sep-1998	5,807,649
FE-00122	US G Electrostatic Discharge Protection For Silicon-On-Insulation	Granted <i>Iation</i>	06-Mar-1997	812,184	04-May-1999	5,901,148
FE-00124	Usal Mode Telephone Handset Satellite Telephone Handset -	Granted	06-Mar-1997	812,183	07-Mar-2000	6,034,399
FE-00124-1	US FE-00124-1 Satellite Telephone Handset	Granted	27-Mar-1997	29069642	28-Sep-1999	D414,486
FE-00126	US Secure Data Transmission on A TDM Isochronous Network	Pending vork	27-Aug-1999	384,429		
	Sn .	Granted	14-Apr-1997	837,165	19-Oct-1999	5,970,095

C
~
_
5
9
•
=<
ø
٩.

CaseNumber Title FE-00130 Impr	er Title Country Status File Date A, Improved Control Telemetry Sienal Communication System For Governiance, Such East	Country Status	Status For Genetal	File Date	File Date ApplNumb	Issue Date	Issue Date PatNumber
				manno Cumica	3		
		NS	Pending	27-Jun-1997	884,675		
		SN	Pending	23-Dec-1999	864,675		
FE-00131	Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture	. (МСD/M,		•			
		SN	Pending	25-Jul-2000	625,641		
		ns	Granted	27-Jun-1997	884,650	02-Feb-1999	5,867,479
		SN	Granted	01-Feb-1999	241,313	18-Jul-2000	6.091.704
FE-00144	Dual Mode Collision Avoidance System					•	
		SN	Abandone				
FE-00165	Radiation Hardened Six Transistor Random Access Memory and Memory Device	rzomory Stemow	and Memor	w Device			
				2000			
		SN	Abandone	04-Jun-1998	090,946		
		SN	Granted	05-Jun-1999	325,645	29-Aug-2000	6,111,780
		WO	Pending	04-Jun-1999	US99/12442		
FE-00170	Enhanced TRENCH Isolation (STI) Method for Fabricating Radiation-Tolerant Integrated Circuit Devices.	ahricating	Radiation-T	olerant Integr	ated Circuit De	evices.	
		Sn	Pending	30-Jun-2000	512.671		
FE-00172	High Accuracy Fabrication Of X-Ray Masks With Optical And E-Beam Lithography	ı Optical A	pu				
		ns	Granted	04-Jun-1996	663,826	26-May-1998	5.756.234
FE-00185	Integrated Circuit Package and Method Increasing Density Of 1/0 Leads	ıg Density	Of I/O Lead	×			
		ns	Pending	16-Jan-1998	007,980		

CaseNumber Title	er Title	Country Status	Status	File Date	File Date ApplNumb	Issue Date	PatNumber
FE-00221	Distributed Determination of Explicit Rate in an ATM Communication System	4TM Conn	munication S	)sstem	:		
		Sn	Expired	03-Jun-1999	60/137,595		
		ns	Expired	19-Oct-1999	60/160,302		
		ns	Pending	12-May-2000	570,050		
FE-00228	Elimination of Narrow Device Width Effects In Complementary Metal Oxide Semiconductor (CMOS) Devices	mplemen	tary Metal O.	xide Semicona	heetor (CMOS) L	)evices	
FE-00233	US Reversible Keypad And Display For A Telephone Handset	us Handset	Unfiled				
FE-00239	US Recessed Gate Process For Silicon-On-Insulator Devices	us Devices	Granted	12-Dec-1997	989,463	18-Apr-2000	6.052,606
FE-00258	US Abandone 04-Nov-1 Shallow Isolation Trench Forming Process For Silicon-on-Insulator Technology	us Ticon-on-1	Abandone Insulator Tec	04-Nov-1997 Imology	964,022		
FE-00275	US Pending 09-Dec- Cold Spare and Voltage Interoperable Off-Chip Driver and Associated Methods	us Priver and	Pending Associated A	09-Dec-1997 <i>1ethods</i>	907,016		
FE-00276	US Pending 05 US Expired 03 Sel∫ Equalized Low Power Precharge Sense AMP For High Speed Memory	us us For High	Pending Expired Speed Memo	05-May-2000 02-Jun-1999 <i>ო</i> კ <sup>,</sup>	566,178 60/137,174		
		sn Sn Us	Pending Expired Expired	. 12-May-2000 10-Feb-2000 01-Jun-1999	570,064 60/181,559 60/137,224		

CaseNumber Tide FE-00277 A Me	mory Device Having Reduced Power Requir	Country Status ements And Associate	File Date ed Methods	File Date ApplNumb thòds	Issue Date	Issue Date PatNumber
FE-00278	US Pending 26-May-199 A Memory Device Having A Chip Scleet Speedup Feature and Associated Methods	s Pending Hure and Associal	26-May-1999 ed Methods	320,227		
FE-00279	US Pending Single Event Upset Hardened CMOS Latch Circuit With Fast Write Time	s Pending Tith Fast Write Tin	26-May-1999 11 <i>e</i>	320,207		
FE-00291	US Multi-Channel Overvoltage Protection Circuit	Abandone	07-Oct-1998	168,430	,	,
FE-00295	US Granted 26-Feb-1998 Method For Fabricating Resistors Within Semiconductor Integrated Circuit Devices	Granted Stor Integrated Ci	26-Feb-1998 rcuit Devices	030,902	03-Oct-2000	6,127,879
FE-00300	US US In Situ Proximity Gap Monitor For Lithography	Pending Expired	25-Jan-2000 01-Feb-1999	491,230 60/118,049		
FE-00319	US Pending 10-Feb-2000 502,062 US Expired 24-Sep-1999 60/155,571 Enhanced Local Oxidation of Silicon (LOCOS) Method for Fabricating Radiation-Tolerant Integrated Circuit Devices	Pending Expired nd for Fabricating	10-Feb-2000 24-Sep-1999 Radiation-Tole	502,062 60/155,571 2rant Integratea	d Circuit Devic	sə
	SN	Unfiled				

CaseNumber Title FE-00320 Enha	nced Single Event Upset Immune Latch Circi	untry	Status	File Date	File Date ApplNumb	Issue Date	PatNumber
FE-00321	US Pending 11-Jan-2000 480,454 WO Pending 11-Jan-2000 US00/00557 US Expired 28-Jul-1999 60/145,939 Method and Apparatus for Hardening A Static Random Access Memory Cell From Single Event Upsets	us wo us dom Acee	Pending Pending Expired	11-Jan-2000 11-Jan-2000 28-Jul-1999 Cell From Sin	480,454 US00/00557 60/145,939 Igle Event Upsets		
		US DE GB FR	Pending Pending Pending Pending	17-Nov-1999 17-Nov-1999 17-Nov-1999 17-Nov-1999	441,941 US99/27302 US99/27302 US99/27302		
FE-00324	US Abandone 28-May-1999 607 Method For Improving Radiation Tolerance of Semiconductor Integrated Circuit Devices	US , iconducto	Abandone Y' Infegrafea	28-May-1999 I Circuit Devic	60/136,480 .c.s		
FE-00352	US US Method and Apparatus for a SEU Tolerant Clock Splitter		Pending Expired	22-Jun-2000 22-Jun-1999	60/139,897	•	
FE-00354	US US Method and Apparatus for A Scannable Hybrid Flip Flop		Expired Pending	30-Apr-1999 28-Apr-2000	60/131,926 559.661		
		US P WO P US E	Pending Pending Expired	28-Apr-2000 (28-Apr-2000 (30-Apr-1999 (6	559,660 US00/11348 60/132,121		

pplNumb Issue Date PatNumber	307,126 Flip-Chip Interconnects	321,565	US00/01356 449,723 60/171,589	563,197 60/137,739	US00/11887 60/164,343 60/140,361
File Date ApplNumb	07-May-1999 30 Vire Bond and F	28-May-1999 32	20-Jan-2000 US 24-Nov-1999 44 23-Dec-1999 60	02-May-2000 5G: 02-Jun-1999 6O/	22-Jun-2000 US00/11 09-Nov-1999 60/164,3 23-Jun-1999 60/140,3
Country Status d Lithographic Masks	Pending ! Using Both H	Pending MOS Latch		ling ed	Pending Expired Expired
ber Tide Pattern Density Tailoring For Etching of Advance	US Pending 07-May-1999 307,126 Method and Apparatus For Evaluating A Known (hood Die Using Both Wire Bond and Flip-Chip Interconnects	US Pending Single-Event Upset Hardened Reconfiguration Bi-Stable CMOS Latch	WO Pending US Pending US Abandone Method and Apparatus for a Voltage Rexponsive RESET for EEPROM	US Pend US Expir Low-Power (MOS Device and Logic Gates/Circuits Therewidth	OM .
CaseNumber Title FE-00371 Patte	FE-00372	FE-00375	FE-00385	FE-00387	

CaseNumber Title FE-00391 Singl	e Event Upset (SEU) Hardened Static Rando	Country Status w Access Memory	Status emory Cel		File Date ApplNumb	Issue Date	PatNumber
	sn ·		Expired	28-May-1999	60/136.479		
	SN		Pending	17-Nov-1999	441.942		
	SN		Pending	30-Aug-2000	651,155		
	Ep	<u>د</u>	Pending	17-Nov-1999	US99/27301		
F.E-00397	Circuit and Method For Limiting Inrush Current Through A Mosfet Circuit and Method For Limiting Inrush Current Through A Transistor/102	ough A N	fosfet ransistor/	102			
	SN	S	Expired	30-Dec-1999	60/174,059		
	OM		Unfiled		•		
	sn ·	S	Pending	12-Jun-2000	591,958		
r. t 00.598	Integrated Resistor Having Aligned Body and Contact and Method for Forming The Same	t and Me	thod for F	orming The Sa	me		
FE-00406	US Storage Unit Subassembly Insertion/Extraction Tool		Provísion	21-Jan-2000	60/178,247		
FE-00410	US Expired 17-Feb-199 Computer Device Having Multiple Linked Parallel Busses and Associated Method	s E. usses and	Expired Id Associale	17-Feb-1999 d Method	60/120,328		
FE-00414	US Pending 14 Self-Restoring Single Event Upset (SEU) Hardened Multiport Memory Cell	s Pa fultiport	Pending 1 Memory C	14-Sep-2000 ell			
	SN		Expired	28-May-1999	60/136,478		
	OM .		Pending	15-May-2000	US00/13095		
	SN		Pending	20-Apr-2000	553,595		

CaseNumber Title FE-00422 Syste	er Title System and Method of Providing-a Spread Spectrum Pulse Width Modulator Clock	Country rum Pulse 1	Status Width Modu	File Date dator Clock	File Date ApplNumb • Clock	Issue Date	PatNumber
FE-00424	US Expired 18-Oc WO Pending 12-An US Pending 12-An Afultiplexor Having A Single Event Upset (SEU) Immune Data Keeper (Treuit	us wo us mmune Da	Expired Pending Pending Ha Keeper (	:t-1999 n-2000 n-2000	60/159,974 USU0/28748 -591,731		
FE-00426	US Pending 08-Jun-2000 Oscillator and Method For Generating A frequency Within A Stable Frequency Range	us cy Within z	Pending 1.Stable Fre	08-Jun-2000 quency Range	589,732		
FE-00431	Method For Testing Known Good Die	ns	Provision	05-Nov-1999	60/163,757	,	
FE-00432	US Pending 24-Jul US Expired 25-Oc Method and Apparatus for a Single Event Upset (SEU) Tolerant Clock Splitter	us us SEU) Toler	Pending Expired ant Clock S	24-Jul-2000 25-Oct-1999 plitter	624,247 60/161,418		
FE-00434	US Expired 30 WO Pending 28 US Pending 28 US Pending 28 Tool Suite for the Rapid Development of Advanced Standard Cell Libraries	us wo us i Standard	Expired Pending Pending	-Apr-1999 -Apr-2000 -Apr-2000	60/131,925 US00/11349 559,659		
FE-00436	US Pending 20-Jun-2000 597,229 A Process For Removing A Silicon-Containing Material Through Use Of A Byproduct Generated During Formation Of A Diffusion Barrier Layer	US Herial Thra	Pending vugh Use Oj	20-Jun-2000 (A Byproduct (	597,229 Generated Duri	ng Formation	Of A
		ns	Unfiled				

CaseNumber Title		Country Status	Status	Fila Data	File Data Amal Mant	7	
FE-00439	Increasing The Susceptability Of Integrated Circuits To Ionizing Radiation	ts To ton	izing Radiatia		amnanddy	tssue Date	raffynmber
		ns	Expired	11-Jun-1999	60/138,718		
		ns	Pending	09-Jun-2000	590,005		
FE-00442	Semiconductor Circuit Having Increased Susceptibility To Ionizing Radiation	ility To L	onizing Radie	tion			
		Sn	Pending	09-Jun-2000	592,4-3		
		ns	Expired	11-Jun-1999	60/138,720		
FE-00443	Semiconductor Device And Circuit Having Low Tolerance To Ionizing Radiation	lerance 1	'o Ionizing Re	ndiation			
	,	SN	Pending	09-Jun-2000	590,806		
		NS	Expired	11-Jun-1999	60/138,721		
FE-00444	Apparatus And Method For Manufacturing A Semiconductor Circuit	conducto	r Circuit				
		ns	Pending	09-Jun-2000	608'065		
FE-00449	Method to Harden Shallow Trench Isolation Against Total Ionizing Dose Radiation	st Total L	onizing Dose				
		ns	Pending	31-Jul-2000			
		NS	Expired		60/146,895		
FE-00450	A New Radiation-Hardened Technique For Preventing Latches From Single Event Upsets	ting Lated	hes From Siny	gle Event Ups	ets		
FE-00451	) Radiation Hardened High Speed Differential Driver	us ,	Provfiled	11-Aug-2000	60/224,649		
		Sn	Expired	20-Jul-1999	60/144,731		

CaseNumber Title FE-00453 Radi	ation Hardened High Speed Differential Recc	Country Status iver	Status	File Date	File Date ApplNumb	Issue Date	PatNum
FE-00456	US Explied 20-Jul-1999 Radiation Hardened Silicon-On-Insulator (SOI) Transistor Having A Body Contact	US ansistor	Expired Having A Ba	20-Jul-1999 nly Contact	60/144,625		
F.E-00458	US Pendi US Expire Circuit For Filtering Single Event Effect (SEE) Induced Glitches	us us hıced Gli	Pending Expired <i>Iches</i>	01-Aug-2000 23-Dec-1999	630,216 60/171,569		
FE-00462	US US WO Method and Apparatus Radiation Hardened Clock Splitter	us us wo Splitter	Pending Expired Pending	30-Aug-2000 07-Sep-1999 06-Sep-2000	651,156 60/152,348 US00/24421	·	
FE-00464	Single Event Upset Immune Oscillator Circuit	Sn	Provision	28-Apr-2000	60/200,348		
FE-00469	US Pending Redundant Oscillator and Method For Generating A Regulated Signal	US A Regula	Pending ted Signal	21-Sep-2000	667,040		
FE-00470	US Pending Controlled Hermetic Solder Sealing For Large Perimeter Components	us imeter Ca	Pending mponents	10-Aug-2000	636,125		
		sn Ns	Abandone Expired	20-Jan-2000 18-Jan-2000	60/177,234 60/176,574		

CaseNumber Title FE-00471 Integ	er Title Integrated Circuits Containing Transistors Operable With Two Power Supply Voltages	Country Status ble With Two Pow	Status wo Power Su	File Date pply Voltage:	File Date ApplNumb y Voltages	Issue Date	PatNumber
FE-00475	Voltage Step-Up Output Buffer With Low Stress	sn sn	Unfiled Proviiled	11-Aug-2000	60/224,650		
FE-00476	U Structured Login After Satellite Service Interruption	Sn ""	Expired	30-May-2000	60/207,913		
FE-00480	Self-Oscillating Switching Regulator	Sn	Expired	18-Jan-2000	60/176,606	٠	
FE-00481	A Radiation Tolerant Storage Array Sense Latch	ns	Pending	03-Oct-2000			
FE-00483	us Polyphase-DFT Sub-band Definition Filtering Architecture		Provfiled	11-Aug-2000	60/224,648		
FE-00486	US Provision t Use of Chalcogenide For Programming Fuses In RAM's or Other Devices	US AM's or C	Provision Uher Devices	11-Feb-2000	60/181,512		
FE-00489	Direct Chip Attach Micro-CGA	Sn	Provision	02-May-2000	60/201,122		
		Sn	Unfiled				

Single Event Upset Immune Lagic Family.  US  A Sense Amp Scheme Hardened for Dynamic Single Event U,  US  Remote Pictures  US  Reduced Stress Interface Column Grid Array  US  Remote Sonar Buoys  US	Kad Hard Ring Oscillator			:	issue Dale - Fallyumber
US  A Sense Amp Scheme Hardened for Dynamic Single Event U,  US  Remate Pictures  US  Reduced Stress Interface Column Grid Array  US  Remote Sonar Buoys  US		Unfiled			
sn sn sn	US US dened for Dynamic Single E	Provision Unfiled	12-May-2000	60/203,895	
US Reduced Stress Interface Column Grid Array US Remote Sonar Buoys US US	Sn .	Provision	06-Jun-2000	60/209,665	
Nemote Sonar Buoys  Wethod For Advanced Fill Pattern Creation		Uniiled			
US Method For Advanced Fill Pattern Creation	ន្តហ	Unfiled	·		
		Unliled			
US Ur FE-00513 Power Conservation Circuit Using The "Seebeck" Effect	US nit Using The "Seebeck" Effe	Unfiled c/			
ru su	sn	Unfiled			

CaseNumber Title FE-00515 Meth	od Of Forming and Applications of Micropip	Country Status es and Chalcoger	s File Date ApplNumb	ıb İssue Date	PatNumber
FE-00516	Fault Isolation Test Methodology	Unfiled			
FE-00521	US Unlited Novel High-Density High-Performance CMOS SRAM Cell Design	US Unliled IM Cell Design			
FE-00522	US Unliled Novel CMOS SRAM Cell Design with Prescribed Power-On Data State US	US Untiled Power-On Data State	State 2000 60/220,700	•	
FE-00527	Solder Column Attach	Open			
FE-00527	On-Chip High Speed Termination	Open			
FE-00528	An Institute Radiation Action of Integrated Circuits	Open			
FE-00539	Visitor Information System (VIS)	Onen		·	
FE-00540	Small Area Sidewall Rapier Contact For Chalcogenide Memory Device	ride Memory Do	evice		
FE-00542	EGA to CGA Conversion Process .	Open			¥
	, ==£	Open			
Tuesday, November 21, 2000	mber 21, 2000	Page 20 of 20			